Amendments to the Claims

This listing of claim will replace all prior versions and listings of claim in the application.

1) (currently amended) A circuit, comprising:

a clock circuit capable of generating a clock signal in response to an adjustable phase step-size; and

a sampler, coupled to the clock circuit, capable of receiving, in response to the clock signal, a data signal having a variable data bit-rate,

wherein the circuit includes at least four stages, each having a respective stage output, wherein the clock circuit includes stall logic capable of holding the third and fourth stage outputs in response to the first and second stage outputs.

2) (original) The circuit of claim 1, wherein the clock circuit includes a phase adjust step-size logic capable of outputting an adjustable magnitude of the phase step-size in response to the variable data bit-rate.

3) (original) The circuit of claim 1, wherein the phase adjust step-size logic is capable of outputting an adjustable direction of the phase step-size in response to the variable data bit-rate.

4) (cancelled)

5) (currently amended) The circuit of claim 1 4, wherein the circuit comprises 6 pipeline stages.

6) (original) The circuit of claim 1, wherein the variable data bit-rate is from approximately 0 parts per million ("ppm") to approximately 5000 ppm.

7) (original) The circuit of claim 1, wherein the adjustable phase step-size is adjusted in response to a first step-size corresponding to data phase drift and a second step-size corresponding to the variable data bit-rate.

8) (original) The circuit of claim 7, wherein the first step size and the second step-size are summed to obtain the adjustable phase step-size.

9) (cancelled)

10) (currently amended) ~~The circuit of claim 9,~~ A circuit, comprising:

a clock circuit capable of generating a clock signal in response to an adjustable phase step-size; and

a sampler, coupled to the clock circuit, capable of receiving, in response to the clock signal, a data signal having a variable data bit-rate,

wherein the clock circuit includes an indicator capable of adjusting the adjustable phase step-size in response to the variable data bit-rate,

wherein the clock circuit includes a counter for obtaining a first step-size and the indicator provides a second step-size, wherein the first step-size and the second step-size are summed to obtain the adjustable phase step-size.

11) (currently amended) The circuit of claim 9, wherein the indicator includes a state machine ~~for~~ capable of detecting the variable data bit-rate.

12) (currently amended) The circuit of claim 1, wherein the clock circuit includes an averaging circuit capable of averaging a plurality of up signals to obtain an average up value and a plurality of down signals to obtain an average down value, and outputting ~~an adjust signal having the selectable~~ the adjustable phase ~~adjust~~ step-size in response to a comparison of the average up value and the average down value.

13) (original) The circuit of claim 1, wherein the circuit is included in a receive circuit coupled to a transmit circuit capable of transmitting the data signal.

14) (currently amended) A circuit, comprising:

a clock circuit capable of generating a clock signal in response to a phase adjust signal;

a sampler, coupled to the clock circuit, capable of receiving, in response to the clock signal, a data signal having a variable data bit-rate; and,

wherein the clock circuit comprises,

a first stage, coupled to the sampler, capable of ~~outputing~~ outputting a first stage output signal in response to ~~the~~ a sampled data signal;

a second stage, coupled to the first stage, capable of outputting a second stage output signal in response to the first stage output signal;

a third stage, coupled to the second stage, capable of outputting the phase adjust signal in response to the second stage output signal; and,

stall logic, coupled to the first, second and third stages, and capable of holding the phase adjust signal in response to the first and second stage output signals.

15) (original) The circuit of claim 14, wherein the first and second stages are successive stages.

16) (original) The circuit of claim 14, wherein the first and second stages are included in a phase detector.

17) (original) The circuit of claim 14, wherein the third stage is included in a phase adjust controller.

18) (currently amended) A circuit, comprising:

a clock circuit capable of generating a clock signal in response to a phase adjust signal having an adjustable step-size; and,

a sampler capable of receiving, in response to the clock signal, a data signal having a variable data bit-rate;

wherein the clock circuit includes,

a first stage, coupled to the sampler, capable of outputting a first stage output signal in response to ~~the~~ a sampled data signal;

a second stage, coupled to the first stage, capable of outputting a second stage output signal in response to the first stage output signal;

a third stage, coupled to the second stage, capable of outputting the phase adjust signal, having a first step-size, in response to the second stage output signal;

stall logic, coupled to the first, second and third stages, capable of holding the phase adjust signal in response to the first and second stage output signals;

an indicator, coupled to the third stage, capable of outputting a second step-size in response to the variable data bit-rate; and,

a counter, coupled to the third stage and the indicator, capable of outputting the phase adjust signal having ~~an~~ the adjustable step-size ~~responsive~~ in response to the first and second step-sizes.

19) (original) The circuit of claim 18, wherein the first and second stages are successive stages.

20) (original) The circuit of claim 18, wherein the first and second stages are included in a phase detector.

21) (currently amended) The circuit of claim 18, wherein the counter is capable of summing the first step-size and the second step-size to provide the adjustable step-size.~~,~~

22) (currently amended) The circuit of claim 18, wherein the indicator includes a state machine capable of ~~for~~ detecting the variable data bit-rate.

23) (currently amended) The circuit of claim 22, wherein the indicator is capable of outputting a first variable frequency phase step-size ~~responsive~~ in response to a

first variable bit-rate in a first state and capable of outputting a second variable frequency phase step-size ~~responsive~~ in response to a second variable bit-rate in a second state.

24) (original) The circuit of claim 23, wherein the first state transitions to a second state responsive to a difference of a number of up signals to a number of down signals, during a period of time, and a threshold value.

25) (currently amended) A circuit comprising,

a clock circuit configured to generate a clock signal in response a phase adjust signal; and

a sampler configured to receive a data signal in response to the clock signal;

wherein the clock circuit comprises,

an averaging circuit capable to output the phase adjust signal in response to an average up signal, obtained from a plurality of up signals in a predetermined period of time, and an average down signal, obtained from a plurality of down ~~signal~~ signals in the predetermined period of time.

26) (original) The circuit of claim 25, wherein the averaging circuit includes:

a mixer counter capable to output the phase adjust signal.

27) (currently amended) The circuit of claim 25, wherein the averaging circuit includes:

a ~~an~~ ~~accumulator/~~comparator circuit~~, coupled to the mixer counter,~~ capable of ~~incrementing or decrementing~~ adjusting the phase adjust signal ~~responsive~~ in response to a comparison of the average up value and the average down value.

28) (original) The circuit of claim 25, wherein the circuit is included in a receive circuit coupled to a transmit circuit capable of transmitting the data signal.

29) (currently amended) An apparatus, comprising:

a transmit circuit capable of transmitting a data signal ~~having a variable data bit-rate~~; and,

a receive circuit ~~capable to generate~~ capable of generating a clock signal in response to the data signal,

wherein the receive circuit includes,

a sampler capable of receiving the data signal in response to the clock signal; and,

a clock circuit, coupled to the sampler, capable of generating the clock signal in response to a phase adjust signal ~~having an adjustable phase step-size~~, wherein the clock circuit comprises,

an averaging circuit capable of outputting the phase adjust signal in response to an average up signal, obtained from a plurality of up signals in a predetermined period of time, and an average down signal, obtained from a plurality of down signals in the predetermined period of time.

30) (currently amended) A method for tracking a signal ~~having a variable data bit-rate~~, comprising ~~the steps of~~:

receiving the signal;

selecting an update rate; and,

selecting an adjustable step-size for an adjust signal ~~responsive~~ in response to the signal, wherein the selecting includes:

averaging a plurality of up signals to obtain an average up value;

averaging a plurality of down signals to obtain an average down value;

outputting the adjust signal in response to the average up value and average down value.

31) (currently amended) The method of claim 30, wherein the receiving ~~step~~ includes:

sampling the signal in response to the adjust signal.

32) (currently amended) The method of claim 30, wherein selecting an adjustable step-size includes:

determining a first step-size based on ~~the~~ a variable data bit-rate of the signal;

determining a second step-size;

summing the first and second step-sizes to obtain the adjustable step-size.

33) (currently amended) A device, comprising:

a sampler capable of obtaining a signal ~~having a variable data bit rate~~ in response to a clock signal; and,

means for adjusting the clock signal in response to a phase adjust signal ~~the variable data bit rate~~, wherein the means for adjusting includes averaging means for outputting the phase adjust signal in response to an average up signal, obtained from a plurality of up signals in a predetermined period of time, and an average down signal, obtained from a plurality of down signals in the predetermined period of time.